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Evaluation of Semiconductor Device Analysis Using the NET-2 Computer Program

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EVALUATION OF SEMICONDUCTOR DEVICE ANALYSIS USING THE NET-2 COMPUTER PROGRAM

Final Report

by

J. P. Raymond and M. G. Krebs

October 1972

This work was sponsored by the Defense Nuclear Agency under Nuclear Weapons Effects Research Subtask TC-022.

United States Army Materiel Command
HARRY DIAMOND LABORATORIES
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13. ABSTRACT

An evaluation of the capability of the NET-2 Circuit/System Analysis Computer Program to perform analysis of radiation effects on complex semiconductor devices and microcircuits is presented. The mathematical models considered include both the terminal built-in models and Linvill lumped models of bipolar and MOS devices. Computations of electrical performance and transient radiation-induced response are performed and compared to available exact results. The derivation of complex models for the elements of a junction-isolated bipolar microcircuit (including the multiple emitter transistor) is demonstrated as well as the analysis of a complete junction-isolated TTL Gate microcircuit. NET-2 capabilities in terms of computer run times, numbers of circuit elements allowed, and accuracy of solution are discussed. Device analysis examples include a p-n junction diode and an intrinsic lumped model p-n-p transistor.

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SECTION 1.0

INTRODUCTION

1.1 Objective

The objective of this program was to evaluate the capability of the NET-2 Circuit/System Analysis Computer Program[1] as an aid in the analysis of radiation effects on complex semiconductor devices and microcircuits. Mathematical models considered included both the terminal built-in models and lumped models of bipolar and MOS devices. The evaluation included the definition of each model in terms acceptable to the CDC 6600 version of NET-2, computation of the electrical performance and transient radiation-induced response, comparison of the calculated results to "exact" solutions when possible to determine accuracy, and comparison of program execution time to calculations with other models to judge the computational efficiency.

1.2 Technical Approach

There are many semiconductor device analysis techniques, models, and computer programs to aid in the numerical analysis. The device models and elements provided in NET-2 allow the convenient use of greater detail and accuracy in simulation than that allowed in other circuit analysis programs (e.g., CIRCUS, SCEPTRE, SYSCAP). This capability is not as complete as that available in special-purpose computer programs (such as those developed by BTL and IBM), but, unlike the device analysis programs, enables simulation of the device under fully general circuit conditions.

In the evaluation of the NET-2 semiconductor device analysis capability it was first necessary to develop confidence in both NET-2 and the lumped model elements necessary for the generalized device modeling. This was accomplished by first considering the electrical performance and radiation-induced photoresponse of simple devices using familiar first-order mathematical models. The lumped model representations of the device could then be compared directly to familiar results. The next step was to increase the complexity of the simple device models by using more lumped model elements and including effects (such as built-in electric fields) that are generally beyond the scope of the familiar terminal device model. Once the credibility of the NET-2/lumped model technique had been established, study was continued to establish the perspective necessary to suggest rewarding applications of NET-2 to existing analytical techniques. This included the derivation of complex models for the elements of a junction-isolated bipolar microcircuit (including the multiple-emitter transistor) and the analysis of a complete junction-isolated TTL Gate microcircuit.

1 A. F. Malmberg, "NET-2 Network Analysis Program - Preliminary User's Manual," Harry Diamond Laboratories; May 1970.

1.3 Summary of Results

All the lumped model elements (combinance, storance, diffusance, driftance, and carrier generation) can be used with the built-in p-n junction model to simulate the electrical performance, transient ionizing radiation-induced photoresponse, and time-dependent neutron-induced displacement damage effects in virtually any bipolar semiconductor device. In the present study, device operation under conditions of junction voltage breakdown were not considered and some modifications would be necessary in the p-n junction model. The terminal device models evaluated were those for the p-n junction diode, the zener diode, the bipolar transistor, and the MOS transistor, all found to be computable and accurate to the limitations implicit within the model.

Overall impressions on the use of NET-2 were very favorable. Initial convergence, numerical stability, accuracy of the solution and computer running times were all good. Computer time for a "typical" transient response calculation, d-c characterization, or swept frequency response were on the order of 100 seconds for problems involving substantial complexity to the analyst, but modest in terms of the code's capacity (e.g., 25 nodes, 100 elements). The cost trade-off in using the lumped model representation rather than a terminal model appeared to be somewhat independent of the number of lumped model elements used and more dependent on the number of p-n junction models used. It appeared that each p-n junction model and associated lumped model elements was roughly equivalent to a single terminal transistor model. The accuracy of the lumped model can, however, often be much greater than a factor of two better than that obtained with a terminal transistor model.

SECTION 2.0

LUMPED-MODEL TECHNIQUE

The lumped model technique is simply the application of a difference-differential approximation to the partial differential equations describing carrier distribution and motion in a semiconductor. Given a particular semiconductor device, each bulk semiconductor region is characterized in terms of a "network" representing carrier distribution and current throughout the region. The p-n junction models provide boundary conditions for each region relating the carrier density at the edges of the junction to the applied junction voltage. The general lumped model technique proposed by Linvill[2, 3, 4] includes representation of both minority and majority carrier flow by either signal-dependent diffusion or drift. The lumped model representation of NET-2 has been simplified to gain more efficient computability and allows characterization of the semiconductor region by the minority carrier distribution and flow. This is essentially the assumption of space-charge neutrality and is implicit in virtually all bipolar device models.[5]

The principal advantages of the NET-2/lumped model are: 1) direct correspondence to the physical processes and radiation effects of the bulk semiconductor, 2) flexibility in the definition of the model complexity, and 3) compatibility in the engineering analysis of many interconnected devices, circuits, or system blocks.

The elements and parameters of the lumped model are illustrated in Figure 1 for a one-dimensional representation of a bulk semiconductor region. Carrier recombination, storage and generation in each sub-region (lump) are represented by the lumped model combinance (H_c), storance (S_t) and current generator (i_g) elements, respectively. Current flow between lumps by carrier diffusion and/or drift is represented by the current through the diffusance (H_d) and driftance (D_f) elements respectively. It is important to note that the current flow in all elements is defined as positive in the direction of "conventional" current flow. When electrons are the minority carriers, the flow of carriers is then opposite the flow of conventional current.

It is helpful to first just consider the carrier generation and recombination processes in n- and p-type semiconductor as shown schematically in Figure 2. The minority carrier density is specified in terms of the "excess" density, or that value different from the thermal equilibrium. For the k-th lumped region then,

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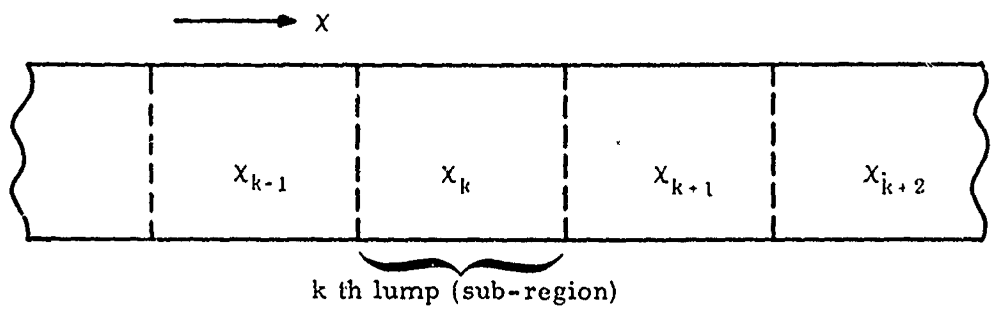
2 J. G. Linvill, "Lumped Models of Transistors and Diodes," Proc. IRE, Vol. 46, pp. 1141-1152; June 1958.

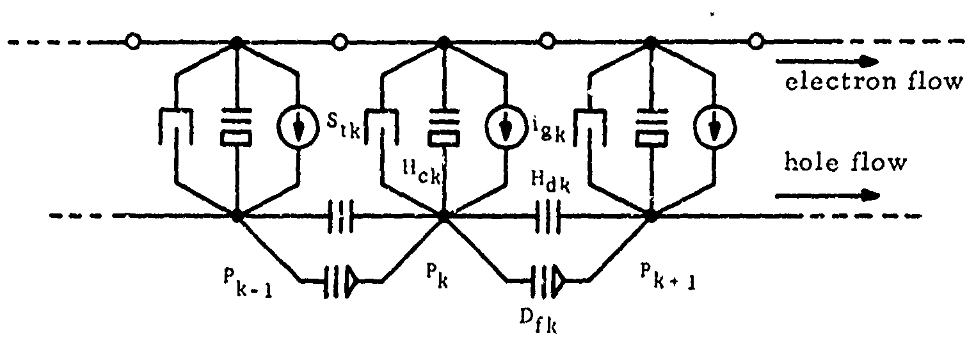
3 J. G. Linvill and J. F. Gibbons, Transistors and Active Circuits, New York: McGraw-Hill Co., 1961.

4 J. G. Linvill, Models of Transistors and Diodes, McGraw-Hill, New York; 1963.

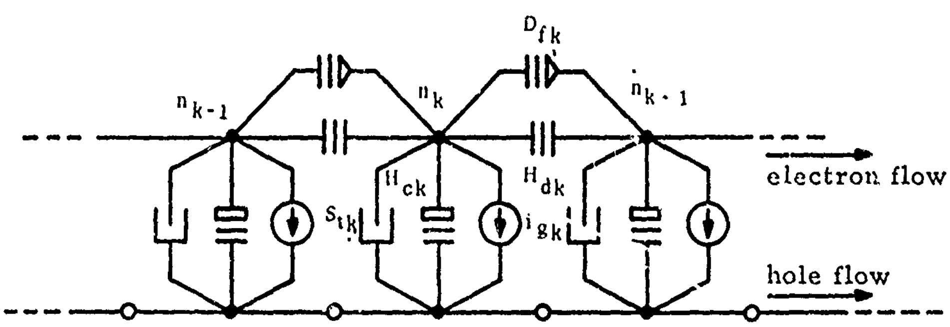
5 J. P. Raymond and R. E. Johnson, "Detailed Lumped-Model Analysis of Transistor Ionizing Radiation Effects," IEEE Trans. Nucl. Sci., Vol. NS-13, No. 6 pp. 95-104; December 1966.



(a) One-dimensional semiconductor region

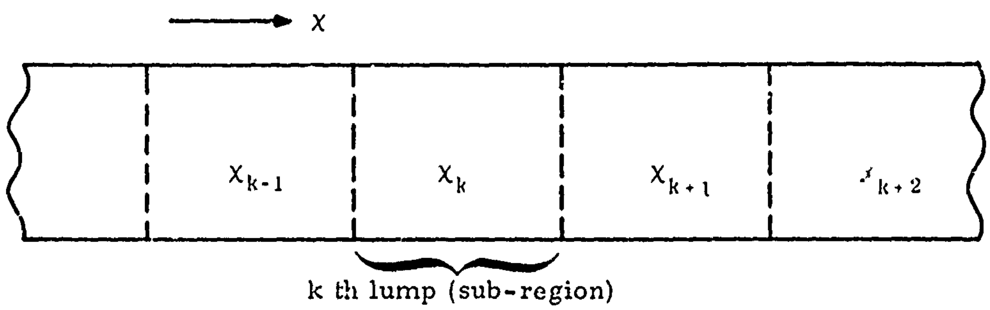


(b) NET-2 lumped model elements: n-type semiconductor

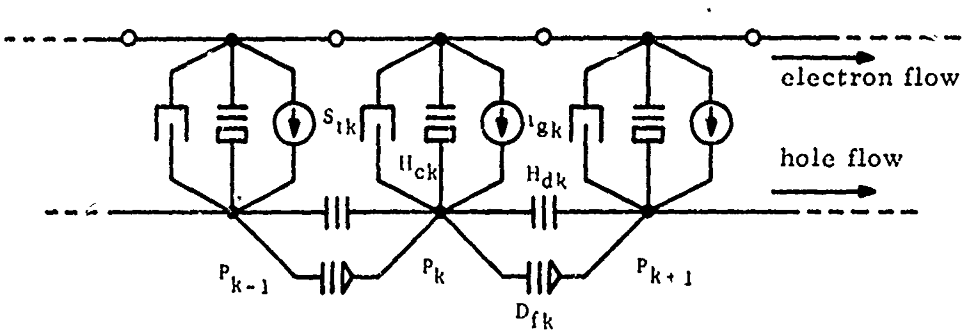


(c) NET-2 lumped model elements: p-type semiconductor

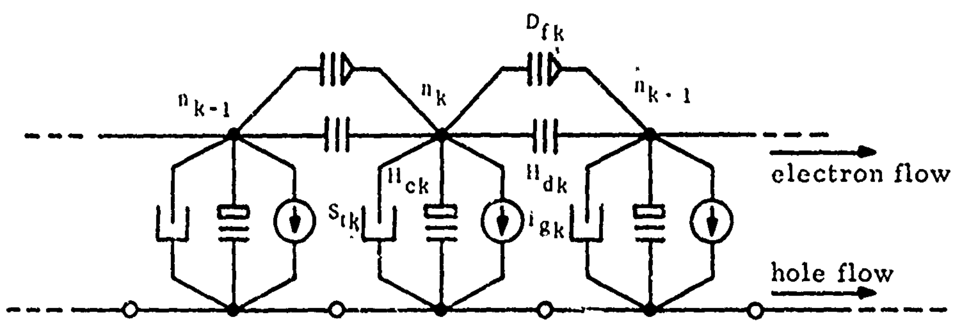
Figure 1 One-Dimensional Lumped Model



(a) One-dimensional semiconductor region



(b) NET-2 lumped model elements: n-type semiconductor



(c) NET-2 lumped model elements: p-type semiconductor

Figure 1 One-Dimensional Lumped Model

$$p_k = P_k - p_n \quad \text{for n-type semiconductor}$$

$$n_k = N_k - n_p \quad \text{for p-type semiconductor}$$

where p_k and n_k are the excess minority carrier densities, P_k and N_k are the actual minority carrier densities, and p_n and n_p are the thermal equilibrium densities. The process of a single event carrier recombination in a semiconductor removes one hole and one electron as free carriers. If the electron density is reconsidered as a negative charge, then the process of recombination is the transfer of a positive charge from the hole side of the combinance to the electron side of the combinance as shown in Figure 2. This reduces the absolute value of both the hole density (a positive number subtracted from a positive quantity) and the electron density (a positive number added to a negative quantity). The carrier recombination rate then is a conventional current flowing from the hole side of the lumped model to the electron side and is given by,

$$i_{r_p} = p_k H_{cp} \quad \text{for n-type semiconductor}$$

$$H_{cp} = qA\Delta W/\tau_p$$

and

$$i_{r_n} = n_k H_{cn} \quad \text{for p-type semiconductor}$$

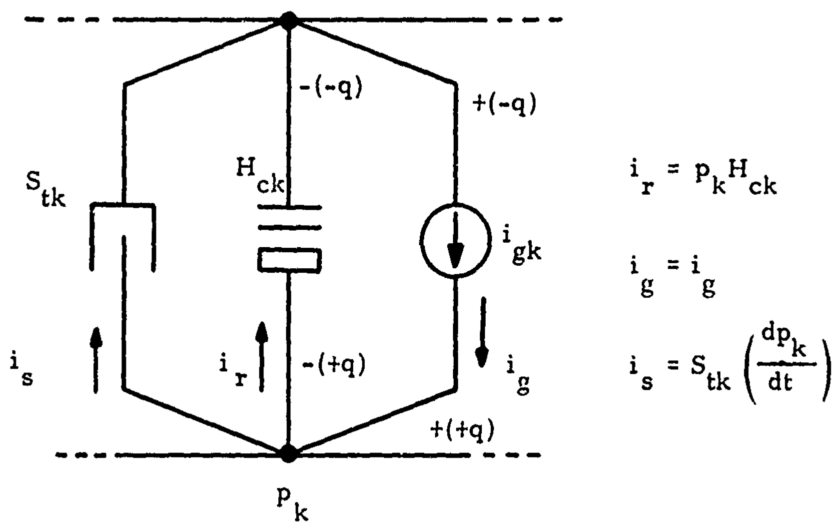
$$H_{cn} = qA\Delta W/\tau_n$$

Physically, this simply represents the average carrier recombination in the lump as proportional to the excess density, proportional to the volume ($A\Delta W$), and inversely proportional to the minority carrier lifetime (τ). Neutron-induced permanent damage effects are included in the lumped model by direct degradation of the minority carrier lifetime or,

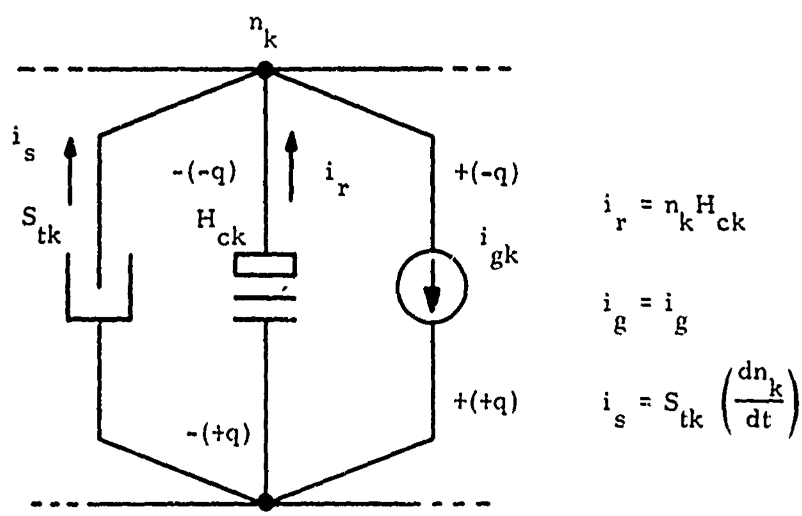
$$\frac{1}{\tau_f}(t) = \frac{1}{\tau_i} + f\left[\Phi(t),\ K(t)\right]$$

where τ_f is the resultant lifetime, τ_i is the initial lifetime, $\Phi(t)$ is the time-dependent neutron fluence, and $K(t)$ is the lifetime damage constant (time-dependent due to short-term annealing effects).

Ionizing radiation effects are represented in the lumped model directly by including the radiation-induced carrier generation in each lump. For high-energy radiation, the ionization will be proportional to the radiation intensity,



(a) n-type semiconductor



(b) p-type semiconductor

Figure 2 Lumped Element Current Definitions and will be absorbed uniformly throughout the device. Since the process of carrier generation is opposite that of carrier recombination, the current generators of the lumped model are in the direction opposite that of the carrier recombination current, as shown in Figure 2. Thus, for both n-type and p-type material we have,

$$i_{gk} = qA\Delta W g_o \dot{\gamma}(t)$$

where $\dot{\gamma}(t)$ is the time-dependent absorbed dose rate.

In addition to representing carrier generation and recombination in each lumped region, we must account for the increase or decrease of carriers under transient conditions. This is represented in the lumped model by storance element (S_{tp} and S_{tn} in Figure 2), which acts much like a capacitance for minority carriers. The current through the storance is given by,

$$i_s = S_{tk}\left(\frac{dp_k}{dt}\right) \quad \text{for n-type semiconductor}$$

$$i_s = S_{tk}\left(\frac{dn_k}{dt}\right) \quad \text{for p-type semiconductor}$$

Carrier transport between lumps is represented by the carrier diffusance, for carrier transport by diffusion, and carrier driftance, for carrier transport as the result of a built-in electric field. The current through the diffusance element is given by,

$$i_{H_d} = (p_k - p_{k+1})\, H_{dk}$$

where $\quad H_d = qAD/\Delta W$

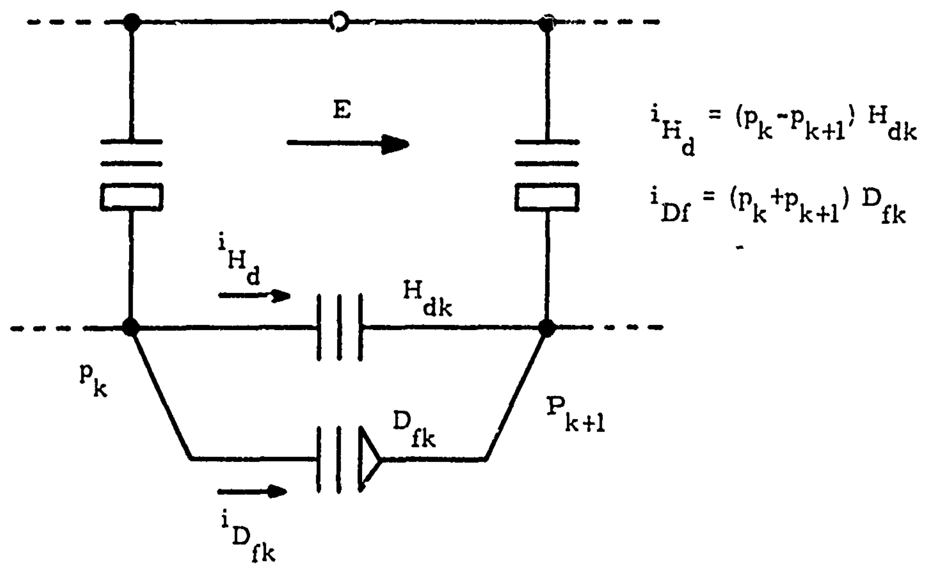
and $\quad D =$ minority carrier diffusion constant

The direction of current flow in the diffusion is shown in Figure 3 for n-type semiconductor and p-type semiconductor. When the minority carriers are electrons, the direction of conventional current flow will be in the direction opposite that of the electron diffusion.

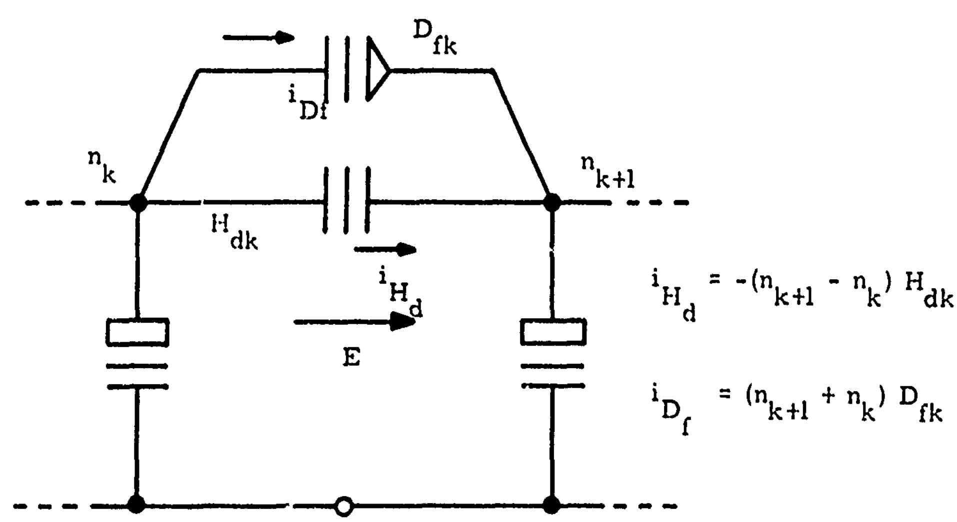
The current through the driftance element is given by,

$$i_{D_{fk}} = (p_{k+1} - p_k)\, D_{fk}$$

where $\quad D_{fk} = qA\mu E$



(a) n=type semiconductor



(b) p-type semiconductor

Figure 3 Transport Lumped Model Elements

μ = minority carrier mobility

E = built-in electric field, positive in the direction of the driftance arrow

It is important to note that the driftance element is oriented in the direction of positive electric field in both n-type and p-type semiconductor. For the p-type semiconductor then, the direction of current through the driftance will be opposite to that of electron flow, <u>and</u> the orientation of the driftance will be opposite to the direction of positive acceleration for the electrons. Current flows through the driftance elements in n-type and p-type semiconductor are shown in Figure 3.

All the lumped model elements available in NET-2 are summarized in Figure 4. The number of lumps used to characterize a bulk semiconductor region of a bipolar device varies from 1 to about 10, depending on the accuracy desired and the degree of variation of built-in electric field and bulk semiconductor parameters through the region. Representations of a single region by a model containing more than 10 lumps is probably not realistic because of the NET-2 numerical accuracy limitations.

Models of each bulk semiconductor region of the device are connected to each other with the built-in p-n junction model, or are connected to the external circuit terminals with an infinite combinance (short-circuit) representing an ohmic contact. The p-n junction model of NET-2 is shown in Figure 5. The minority carrier <u>excess</u> density at the edges of the junction is defined in terms of the applied junction voltage,

$$p_1 = p_n \left[\exp(\theta V) - 1 \right] \quad \text{for the n-side}$$

$$n_1 = n_p \left[\exp(\theta V) - 1 \right] \quad \text{for the p-side}$$

where $\theta = q/kT$ and p_n, n_p are the thermal equilibrium minority carrier densities at the n-type and p-type sides of the junction respectively. Currents through the junction are continuous. That is, the current that enters one side as a minority carrier flow is identical to that leaving the other side of the junction as a majority carrier flow. The depletion capacitance of the junction is connected between majority carrier nodes. Doping levels and grading of the junction determine the zero volt capacitance (C_0), the grade constant n (1/2 for an abrupt junction to 1/3 for a linearly graded junction) and barrier potential, V_z.

The lumped model elements and p-n junction model described enable the NET-2 user to define a wide range of models for many bipolar devices and elements of monolithic integrated circuits. The following discussion

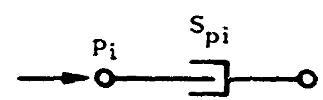
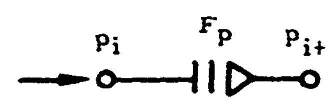
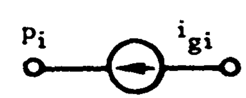
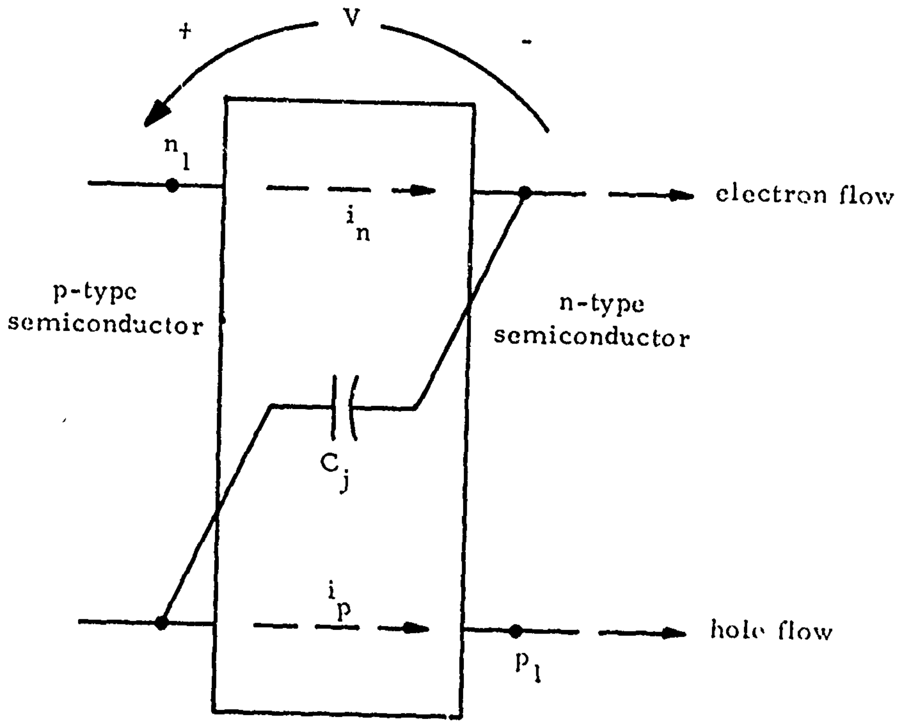
ELEMENT	DEFINITION	SYMBOL	TERMINAL CURRENT
COMBINANCE	$H_{ci} = \frac{qA\Delta x}{\tau_{pi}}$		$i_{H_{ci}} = p_i H_{ci}$
STORANCE	$S_{pi} = qA\Delta x$		$i_{S_{pi}} = S_{pi} \frac{dp_i}{dt}$
DIFFUSANCE	$H_{d_{i,\,i+1}} = \frac{qAD_p}{\Delta x}$		$i_{H_d} = (p_i - p_{i+1}) H_{d_{i,\,i+1}}$
DRIFTANCE	$F_{p_{i,\,i+1}} = qA\mu_p \mathcal{E}$		$i_{F_p} = \left(\frac{p_i + p_{i+1}}{2}\right) F_{p_{i,\,i+1}}$
CARRIER GENERATION	$i_{gi} = qA\Delta x\, g_o \dot{\gamma}$		i_{gi}

Figure 4. Summary of Lumped-Model Parameters



$$n_1 = n_p \left[\exp\left(\frac{qV}{kt}\right) - 1\right]$$

$$p_1 = p_n \left[\exp\left(\frac{qV}{kt}\right) - 1\right]$$

$$C_j = C_o \Big/ \left(1 - \frac{V}{V_z}\right)^n$$

Figure 5. NET-2 P-N Junction Model

(Section 3) presents a summary of the results that lead to the credibility of NET-2/lumped model analysis. Section 4 presents the detailed format (with comments) for two semiconductor device analysis problems that may be helpful to the user as examples.

SECTION 3.0

TECHNICAL RESULTS*

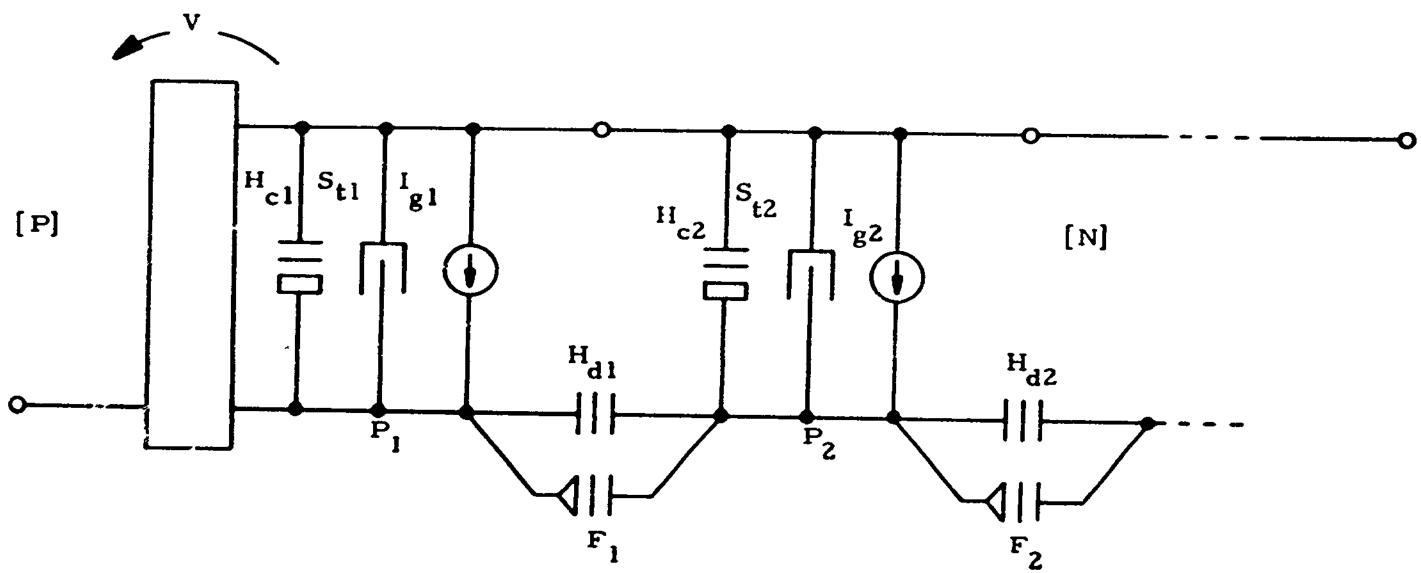
3.1 P-N Junction Diode Analysis

Electrical behavior and photoresponse of an ideal p^+-n diode can be characterized by determining the carrier flow and distribution in the high-resistivity n-region of the diode. The general form of the lumped model diode representation is shown in Figure 6. Combinance and storance elements represent the average of carrier recombination and storage for a finite region of bulk semiconductor. Complex ionizing radiation effects, as observed from the overall device photoresponse, are represented simply as the radiation-induced carrier generation proportional to the time-dependent ionizing radiation absorbed dose rate. Carrier transport between lumped regions by either diffusion or drift is represented in the lumped model by the current through the diffusance and driftance elements, respectively. The lumped model representation of the diode n-region is defined on one side by the p-n junction model, and on the other side by the ohmic contact (or infinite recombination surface). The number of lumps used in the representation and their relative geometry is arbitrary and influences the accuracy of the solution, but cannot add independent parameters necessary to define the diode behavior. The simple 1-lump diode representation is equivalent to the "Ebers-Moll" diode model used as the basis for the NET-2 built-in terminal model. Increasing the complexity of the diode lumped model adds an improved representation of the distributed effects present in the exact solution of diode behavior.

NET-2 calculation of diode small-signal a-c admittance is shown in Figure 7 for the terminal model, 1-lump model, and 2-lump model. Physical parameters are identical in the derivation for all parameters of the three models. By definition, the parameter values of the terminal and 1-lump model were selected to give an identical representation of the diode admittance. As shown in Figure 7, the admittance can be separated into the conductance of constant value. The susceptance, of course, is the reciprocal of the diode diffusion capacitance. The improved accuracy of the 2-lump diode representation demonstrates the effects of distributed carrier density and flow in the admittance at radian frequencies on the order of the reciprocal of the n-region minority carrier lifetime.

More complex effects are involved in the representation of the transient diode photocurrent to a step function of ionizing radiation. The calculated reverse-biased transient photocurrent is shown in Figure 8 using the representations of the 2- and 5-lumped models compared to the error-function solution of the

* Results were reported in "Lumped Model Analysis of Semiconductor Devices Using the NET-2 Circuit/System Analysis Program," by J. P. Raymond, and M. G. Krebs, IEEE Transactions on Nuclear Science, Vol. NS-19, Dec. 1972, pp. 103-107.



$$P_1 = P_{n0}\left[\exp\left(qV/kT\right) - 1\right]$$

Figure 6 General Diode Lumped Model.

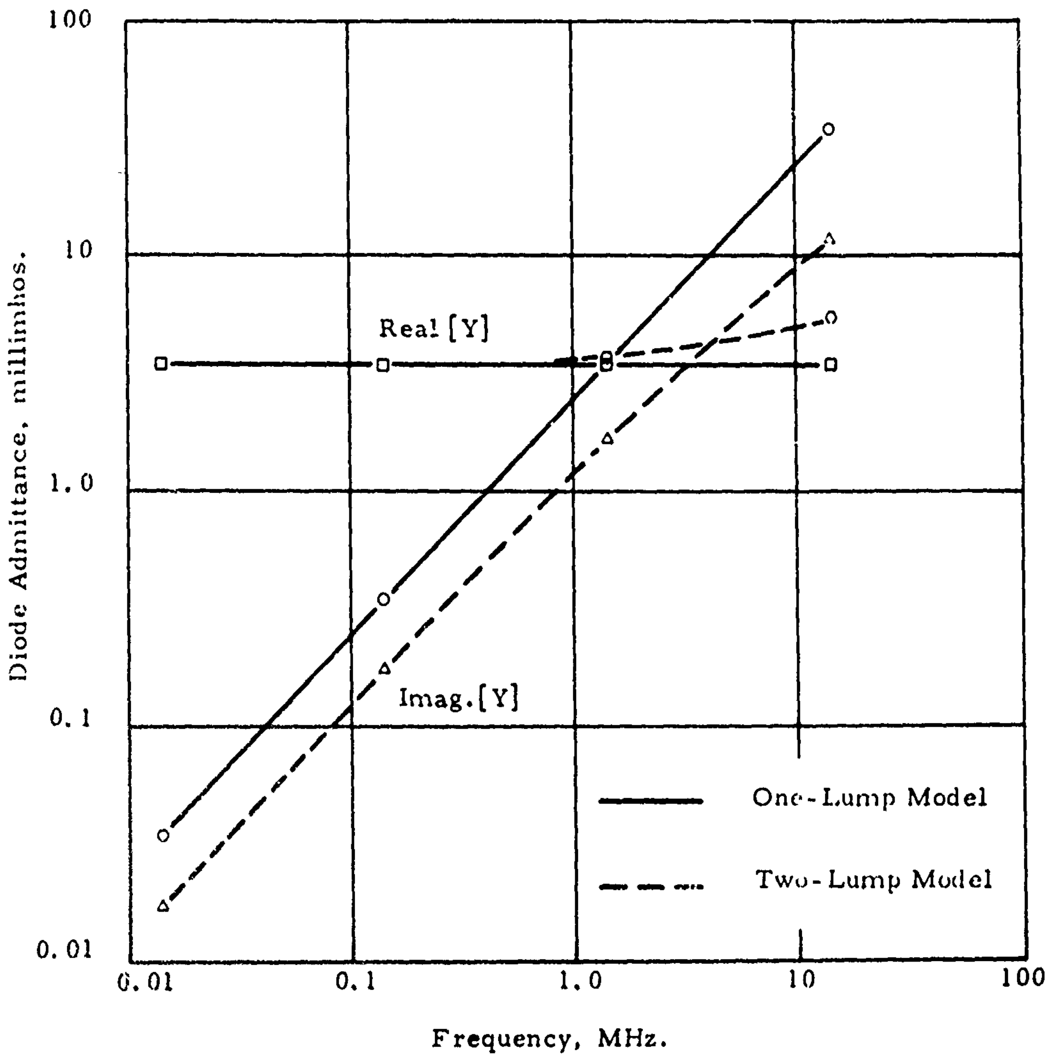


Figure 7 Lumped Model Representation of Diode Forward Admittance.

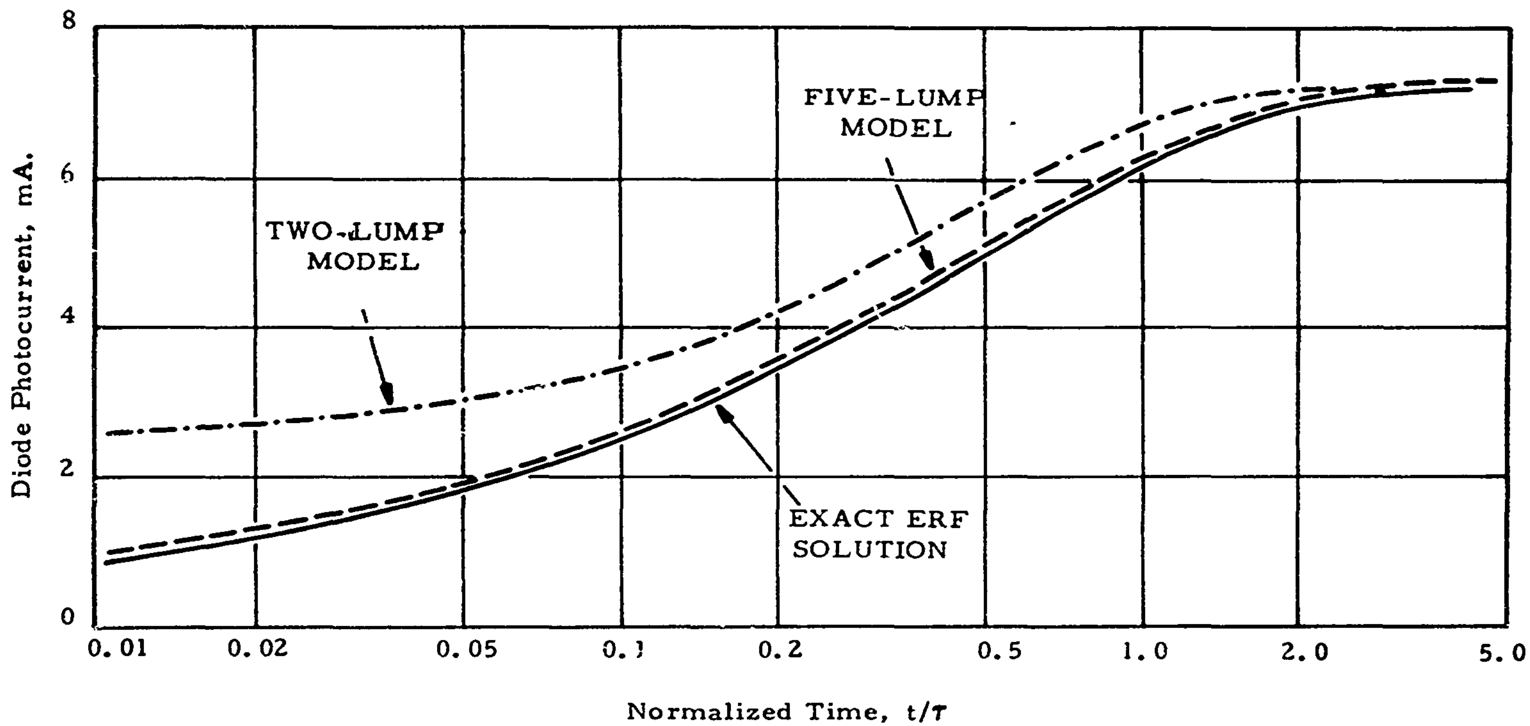


Figure 8 Diode Step Photoresponse.

partial differential equations of radiation-induced carrier distribution and flow. The 2-lump model accurately represents the peak photocurrent observed in a wide radiation pulse (compared to the diode minority carrier lifetime), but is inaccurate in the representation at narrow pulse widths or at short times following the onset of the radiation step function. The 5-lump model also accurately represents the wide pulse photocurrent and shows substantial improvement in the accuracy of the narrow pulse peak photocurrent.

Evaluation of the accuracy of the lumped model as a function of the geometrical approximation and topological detail must include a wide range of diode operating conditions. As an illustration, the worst case error in the calculation of diode recovery time is summarized in Table I for a forward current of 10 mA and a range of reverse currents from 0.1 mA to 20 mA, and lumped models ranging from 2- to 10-lump representations. Increasing the complexity of the model from the 2-lump representation to the 3- or 5-lump representation seems to gain substantially in accuracy, but no substantial gain is obtained by increasing the lumped model from 5 to 10 lumps. The results demonstrate the possible tradeoff between the lumped model representation and a special purpose program designed to numerically solve the device partial differential equations under restricted electrical boundary conditions.

Forward Current = 10mA, Diode n-region Lifetime = 100ns

Lumped Model	Error Range	Reverse Current Range
1-L	18% to 107%	1mA to 20mA
2-L	1.2% to 47%	0.1mA to 20mA
3-L	2.5% to 18%	0.1mA to 20mA
5-L	0.3% to 6.1%	0.1mA to 20mA
10-L	0.1% to 5.5%	0.1mA to 20mA

Table I. Diode Recovery Calculation Worst Case Error

The lumped model can also be used to evaluate the physical effects of a "real" semiconductor device structure. As an example, we can consider the diode recovery time and photocurrent of an epitaxial diode with the built-in electric field of the high-low n-n^+ junction. Diode recovery characteristics have been studied in exact solutions to the diode partial differential equations with the assumption of a constant built-in field and ideal electrical boundary conditions.[6] Solution of the characteristics of a "real" diode would be necessary when it is desired to determine the parameters of a simplified terminal model for simulation of electrical

[6] D. P. Kennedy, "Reverse Transient Characteristics of a P-N Junction Due to Minority Carrier Storage," IEEE Trans. on Electron Devices, Vol. ED-9, No. 2, pp. 174-182; March 1962.

characteristics and photoresponse. Diode electrical recovery times and steady state photocurrent calculated with a 16-lump model are shown in Figure 9 for the fields of both an n^+ -n and n-n^+ diode cathode. In this case, the detail of the lumped model representation is determined primarily by the accurate representation of carrier flow by drift as a result of the built-in field varying throughout the diode.

Computer time required for the diode analysis was not dominated by the complexity of the diode lumped model. Calculation of the field-inclusive 16 lump diode recovery time, for example, was less than twice as expensive as the calculation of the diode recovery time for a 2-lump diode model. Experience with the NET-2 models leads to a rough observation of relative computer time. Each p-n junction of the lumped model seems about equivalent to a simple built-in transistor model. In other words, the computer time for a reasonably complex three-junction device is about that required for a reasonably complex three-transistor circuit. Thus, additional complexity which may be desired for accuracy of simulation can be obtained for a modest increase in running time.

3.2 Bipolar Transistor Analysis

Extension of the analysis to more complex bipolar structures is straightforward. The most familiar lumped model representation of the bipolar transistor is a 1-lump base region between the emitter and collector junction models, and is equivalent to the basic form of the Ebers-Moll model. The equivalence of the two models in NET-2 was verified in the calculation of d-c characteristics, gain as a function of frequency, and large-signal switching transients. Parameters for the basic lumped model and Ebers-Moll model were derived for the same transistor. The equivalence of the lumped model and Ebers-Moll model holds only for the basic lumped model. The complex frequency response of the transistor, for example, can be represented more accurately by a lumped model with several sections in the base region, especially with the influence of a built-in base electric field. This additional accuracy is necessary in representing the reverse-gain characteristics as a function of frequency and the forward gain at frequencies near the common-base gain cutoff frequency, but is not necessary in most transistor simulations. A more accurate representation of the collector region, on the other hand, is necessary to reasonably simulate transistor electrical storage time, active-region photoresponse, and radiation-induced saturated storage time. The junction photocurrent of a uniformly doped collector region is represented in NET-2 by a current source in the Ebers-Moll model whose waveform is based on an approximation to the ideal photocurrent time-dependence for the specified ionizing radiation waveform. The lumped model can, however, be used to represent the photoresponse of non-ideal structures, such as the photoresponse of a transistor with an epitaxial collector and built-in collector electric field.

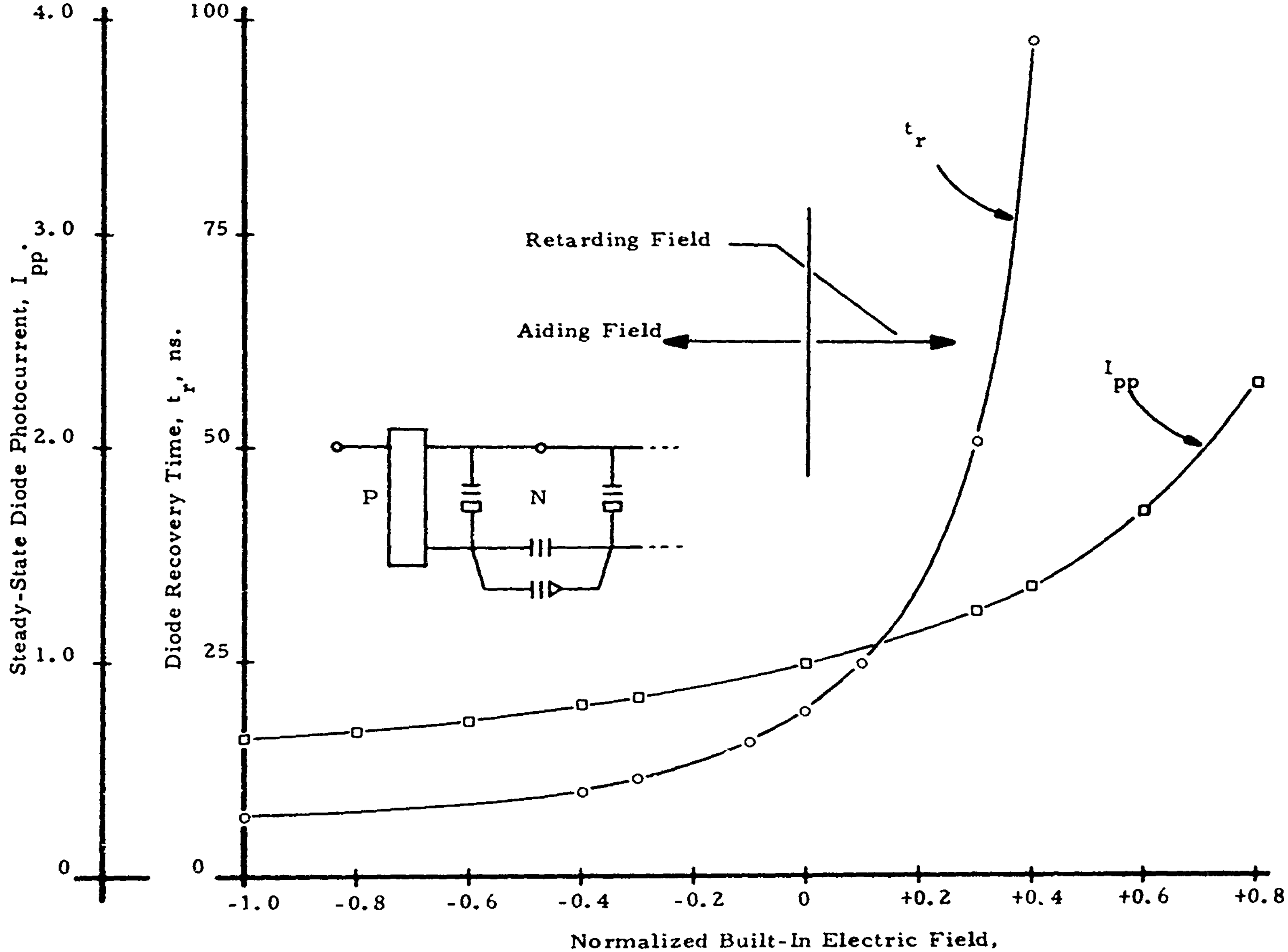


Figure 9 Graded Base Diode Characteristics.

Computability of the lumped model transistor photoresponse is demonstrated by the results shown in Figure 10. Calculated results represent the transient collector current of a transistor inverter for exposure to increasing levels of 2 MeV flash x-ray ionizing radiation pulse. Since the base of the transistor is pulled down to -2 volts through a large (25 kΩ) resistor, the photoresponse at low radiation levels is just the collector primary photocurrent of the transistor. As the radiation level is increased, the primary photocurrent becomes great enough to induce secondary photocurrent. The high level photoresponse shown in Figure 10 illustrates the turn-on delay time, secondary gain multiplication, saturation and saturated recovery time of the collector current. The transistor model had a 1-lump approximation for the base region and a 4-lump graded geometry approximation for the uniformly-doped collector region.

Addition of another p-n junction and bulk semiconductor region extends the transistor model to that of a junction-isolated microcircuit transistor element. In this case, the base region is still a 1-lump representation, and the graded geometry approximation is used for the substrate region rather than for the collector region. The collector region of the transistor element is approximated by four constant geometry regions dividing the bulk collector between the base and substrate p-n junctions. The calculated photoresponse of a microcircuit transistor element in the same inverter circuit is shown in Figure 11. Since the geometry of the discrete and junction-isolated transistors was held constant, the elements could be compared as a microcircuit transistor with and without dielectric isolation. The transient collector photocurrent of the junction-isolated transistor (Figure 11) is greater than that of the discrete transistor at low radiation levels, but not at high radiation levels. The increase is due to the added primary photocurrent of the substrate junction that includes some of the carriers generated in the collector region. This carrier competition then decreases the collector primary photocurrent and the resultant secondary photoresponse when the transistor is turned on.

3.3 TTL Gate Analysis

The analysis of basic one-dimensional diode and transistor structures just described was essential to establish the credibility of the NET-2/lumped-model analysis. The analysis of the actual elements of bipolar planar technology requires definition of the lumped model for two-dimensional multiregion structures. Considerations in deriving these element models and the limitations of NET-2 are presented through the analysis of a transistor-transistor-logic (TTL) gate.

A mathematical model was derived for the junction-isolated TTL gate as the interconnection of detailed lumped models for each of the transistor elements and ideal passive resistor elements. The lumped models of the transistor elements were derived by partitioning each element into several one-dimensional "devices", each with its own lumped model representation. A schematic

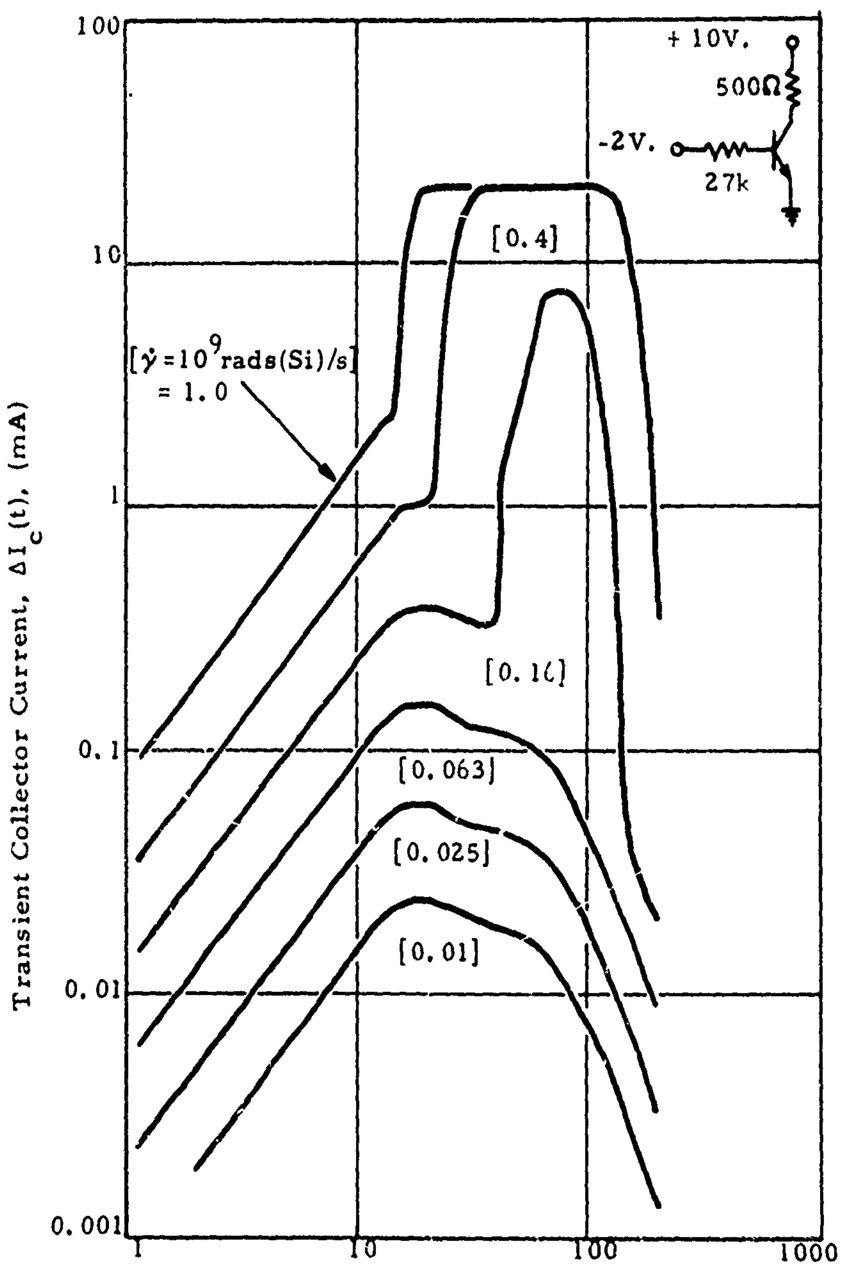


Figure 10 Bipolar Transistor Photoresponse.

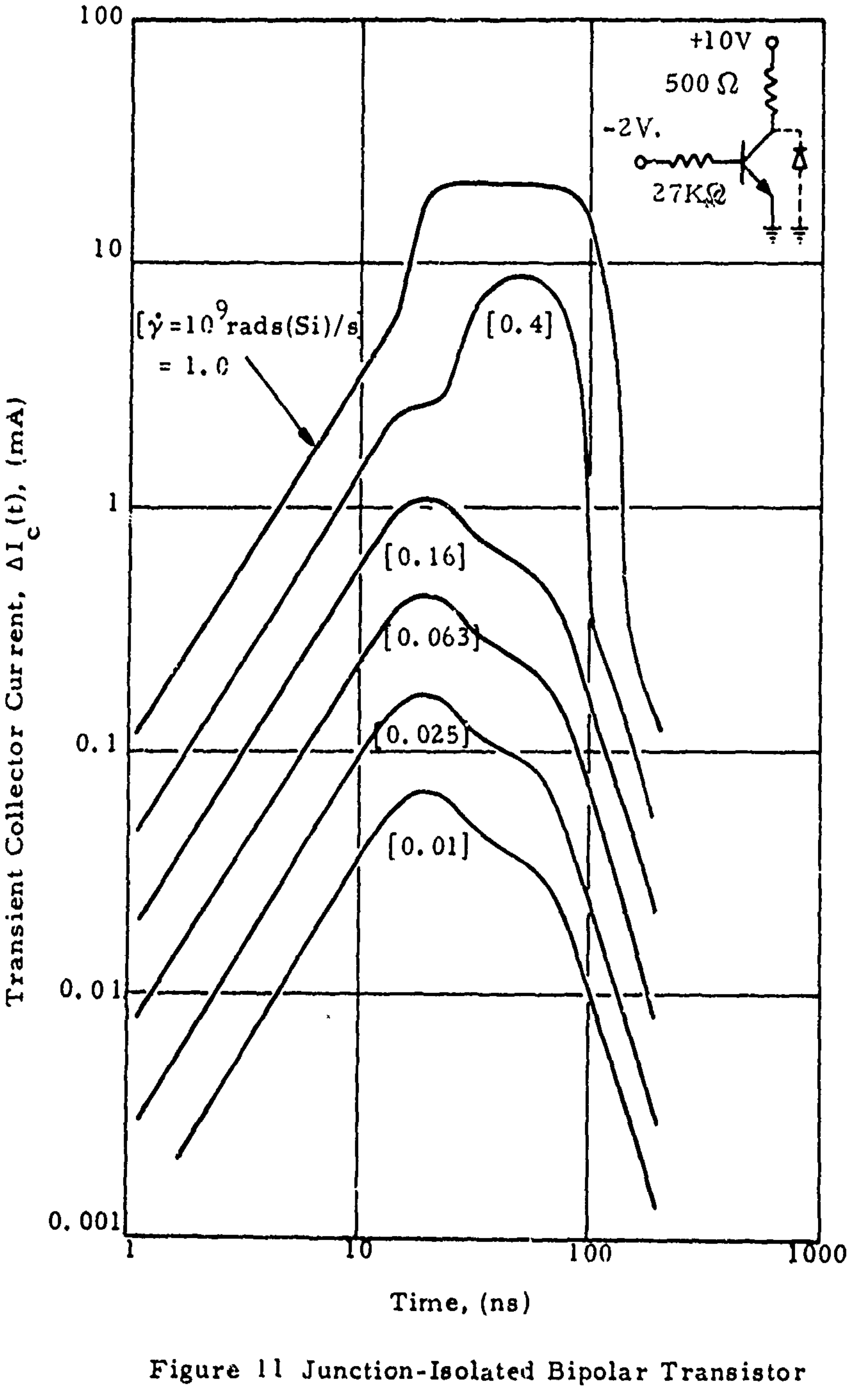


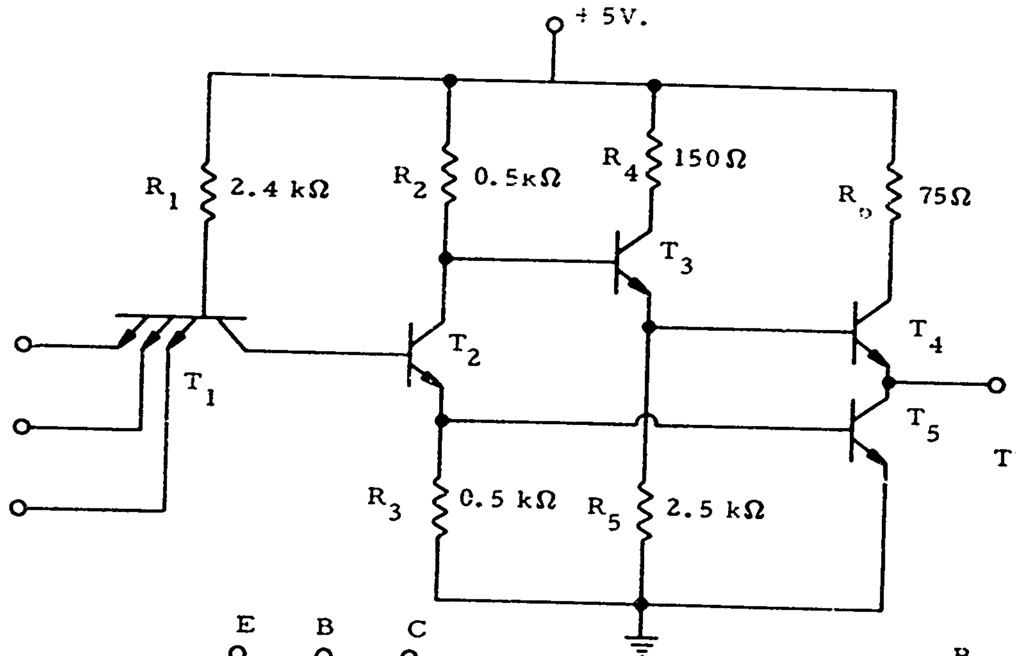
Figure 11 Junction-Isolated Bipolar Transistor Element Photoresponse.

of the TTL gate is shown in Figure 12 with the partitioned geometry of the transistor elements. For the single-emitter transistor, the element is partitioned into 1) a one-dimensional junction-isolated transistor element, 2) a one-dimensional p-n-p "base-overlap" transistor, and 3) a one-dimensional "collector-overlap" n-p diode. The multiple-emitter transistor, in addition, includes separate emitter junctions for each input, and provision for carrier diffusion between contiguous emitters. Specific approximations used for each semiconductor region are listed in Table II. The entire TTL gate model included the specification of 15 p-n junction models (with 6 parameter values each), 5 resistors, 97 diffusance element, 101 combinance elements, 101 storance elements, and 101 current generators representing radiation-induced carrier generation in each lumped region. Fortunately, it was only necessary to derive the lumped model parameters for a single transistor from the basic data on the doping profile and then obtain all other parameter values by scaling to the geometry of each transistor element.

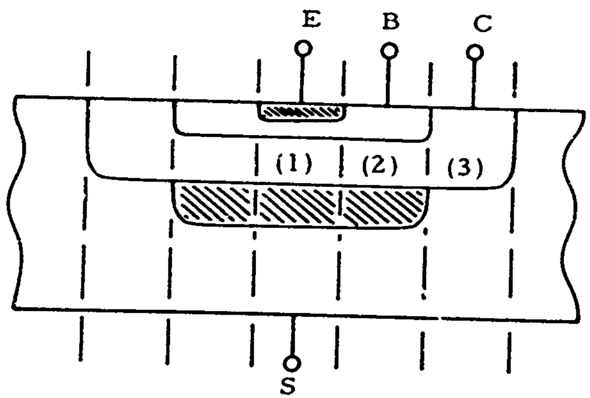
<u>One-dimensional central microcircuit transistor</u>	
Emitter:	one lump, included in base region model
Base:	one lump
Collector -n:	six lumps, linearly scaled
Collector -n^+:	four lumps, linearly scaled
Built-in field at n-n^+ junction:	two elements
Substrate:	four lumps, exponentially scaled
<u>Overlap p-n-p transistor</u>	
Base:	one lump
Collector -n:	six lumps, linearly scaled
Collector -n^+:	four lumps, linearly scaled
Built-in field at n-n^+ junction:	two elements
Substrate:	four lumps, exponentially scaled
<u>Overlap n-p diode</u>	
Collector -n:	four lumps, gradually scaled
Substrate:	four lumps, exponentially scaled

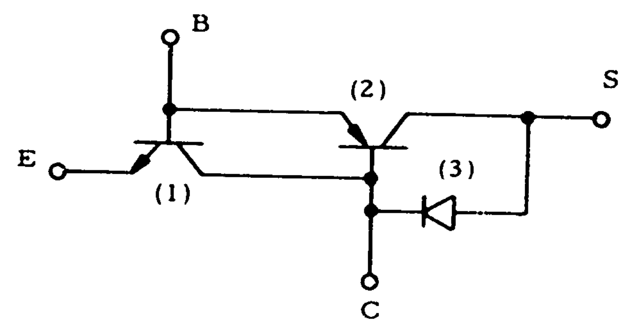
Table II

Approximations Used in Junction-Isolated Transistor Element Models



TTL Gate Schematic





Transistor Element Partitioning

Figure 12 MC507 TTL Gate Schematic and Transistor Definition.

Electrical switching response of the TTL gate was calculated with the full mathematical model without difficulty, and accurately represented the performance of the circuit. Calculation of the TTL gate photoresponse was frustrated by NET-2's limitation on the number of independent current sources. On the CDC 6600/CYBERNET system used, the maximum number of independent sources was determined as approximately 50. This limit is the result of a somewhat arbitrary partitioning of total system capacity and certainly represents a reasonable limit for most problems. In the lumped model, however, radiation-induced carrier generation is represented by a current generator that has the time-dependence of the absorbed radiation pulse and magnitude scaled to the geometry of the lumped region. To solve the problem for the purpose of this illustration, the photoresponse of the TTL gate was computed considering only those photocurrents resulting from carrier generation in the microcircuit substrate and transistor "excess collector" regions. The calculated "OFF" state and "ON" state output photoresponse for a 2 MeV flash x-ray pulse of peak radiation intensity of 2 x 10^9 rads(Si)/s is shown in Figure 13. Calculated results are within a factor of two of the experimental results reported earlier.[7] Improved accuracy would be obtained with additional current sources and diffused resistor models.

The principal objective of the TTL gate analysis was to illustrate the capacity of NET-2 in the detailed analysis of a very complex semiconductor device organized as a circuit connection of more basic elements. Parameters of the model are the doping profile (common to all elements), bulk semiconductor parameters of each region (common to all elements), and the specific geometry of each element. Thus, the analysis of the gate is a rigorous study with a special-purpose computer program. The detailed analysis of the microcircuit can be used as the basis for derivation of a simplified terminal microcircuit model, or as a means of improving the microcircuit device to improve electrical performance, radiation hardness, or both.

[7] J. P. Raymond, "Component Vulnerability of Microcircuits," IEEE Trans. Nucl. Sci., Vol. NS-17, No. 6, pp. 91-95; December 1970.

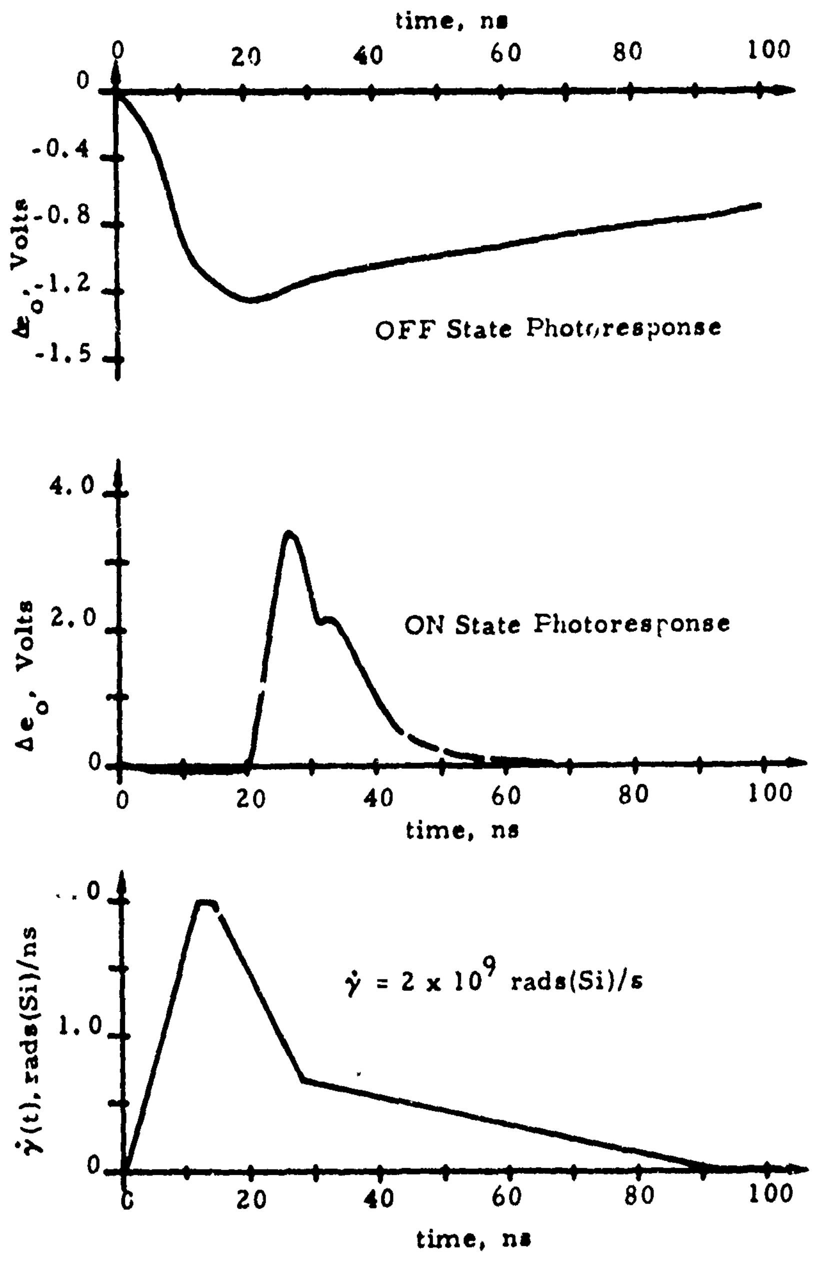


Figure 13 Calculated MC507 Photoresponse

SECTION 4.0

SEMICONDUCTOR DEVICE ANALYSIS EXAMPLES

Two semiconductor device analysis examples are presented to aid the user in setting up problems involving Linvill lumped elements. The first example deals with the geometry definition and problem statement of a 5-lump p-n junction diode photoresponse analysis. The second example presents the analysis of a lumped-model transistor.

4.1 P-N Junction Diode Analysis Example

Figure 14 shows the schematic of a 5-lump p-n diode in a circuit that reverse biases the device. Geometrical parameters for the lumps were selected by using the exponential definition illustrated in Figure 15. The geometrical definition is based on the assumptions that (1) the change in carrier densities from one lump to the next should be approximately equal for all lumps, and (2) that the general form of the solution will be exponential with a characteristic length equal to the minority carrier diffusion length. For the five-lump model then, the edges of each lumped region were selected to fall at equal differences in carrier density across the region. This, with the definition of a total length of the region to be modeled, defines the one-dimensional length of each of the five lumped regions. Boundary conditions on the region shown in Figure 15 are a p-n junction at $x = 0$, and an ohmic contact (or infinite recombination surface) at $x = x_T$.

Figure 16 is a Fortran listing of a computer program which will compute the component values for the pi-section lumps of each semiconductor region. The inputs to the program are 1) the semiconductor junction area, A, 2) the minority carrier lifetime, TAU, 3) the minority carrier diffusion constant, DP, and 4) the number of pi-sections, N. The program computes the minority carrier diffusion length (L), the total length of the semiconductor region (LT), the X location of each node, and the values of combinances, storances and diffusance to be entered into the NET-2 input deck. The program output for the 5-lump example problem is given in Figure 17.

The NET-2 input deck, Figure 18, was set up to compute the unsaturated transient photoresponse in state 1 for a step turn-off of radiation with resistor R1 set to a value of 10 ohms. In state 2, R1 was set to 10k ohms and nine transient responses representing radiation-induced diode saturation and recovery were computed for the given values of parametric variable, P1, a multiplier which scales the size of the input photocurrent step. The plotted results of the run are presented as Figures 19, 20, and 21.

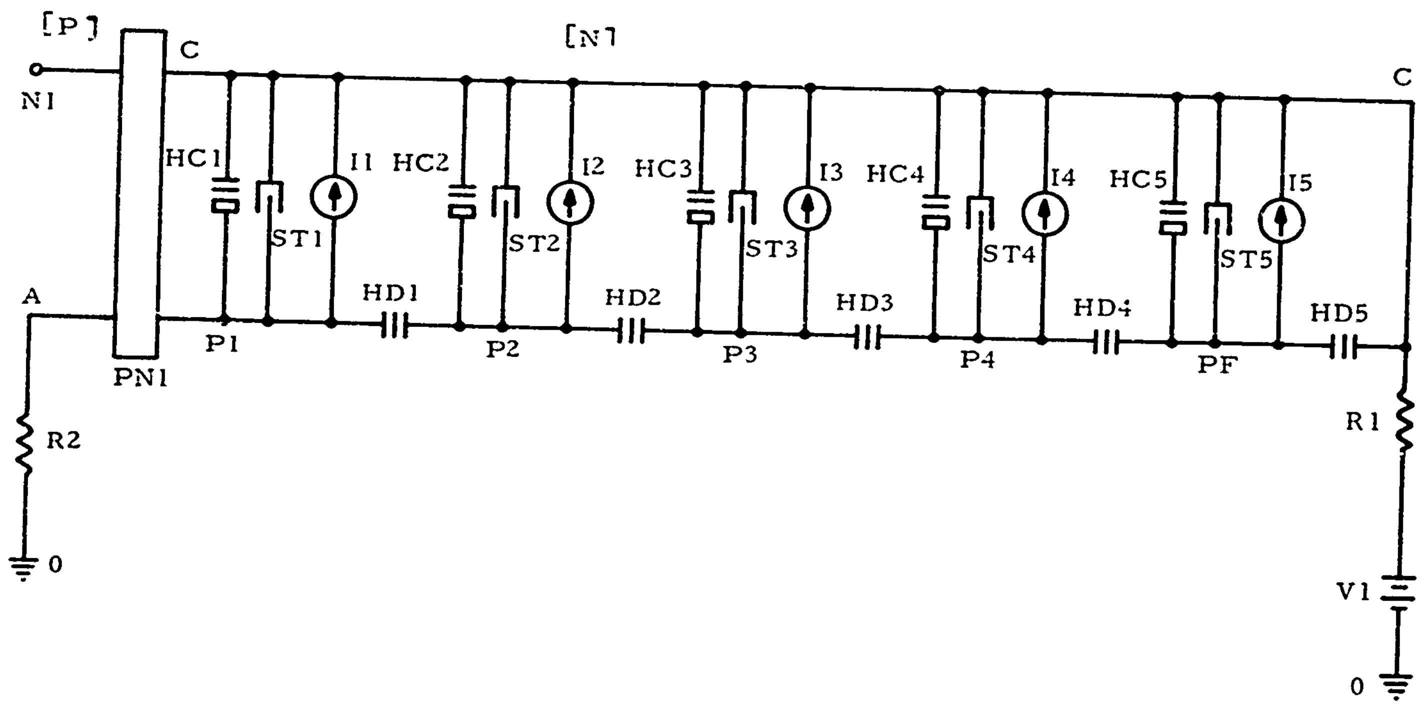
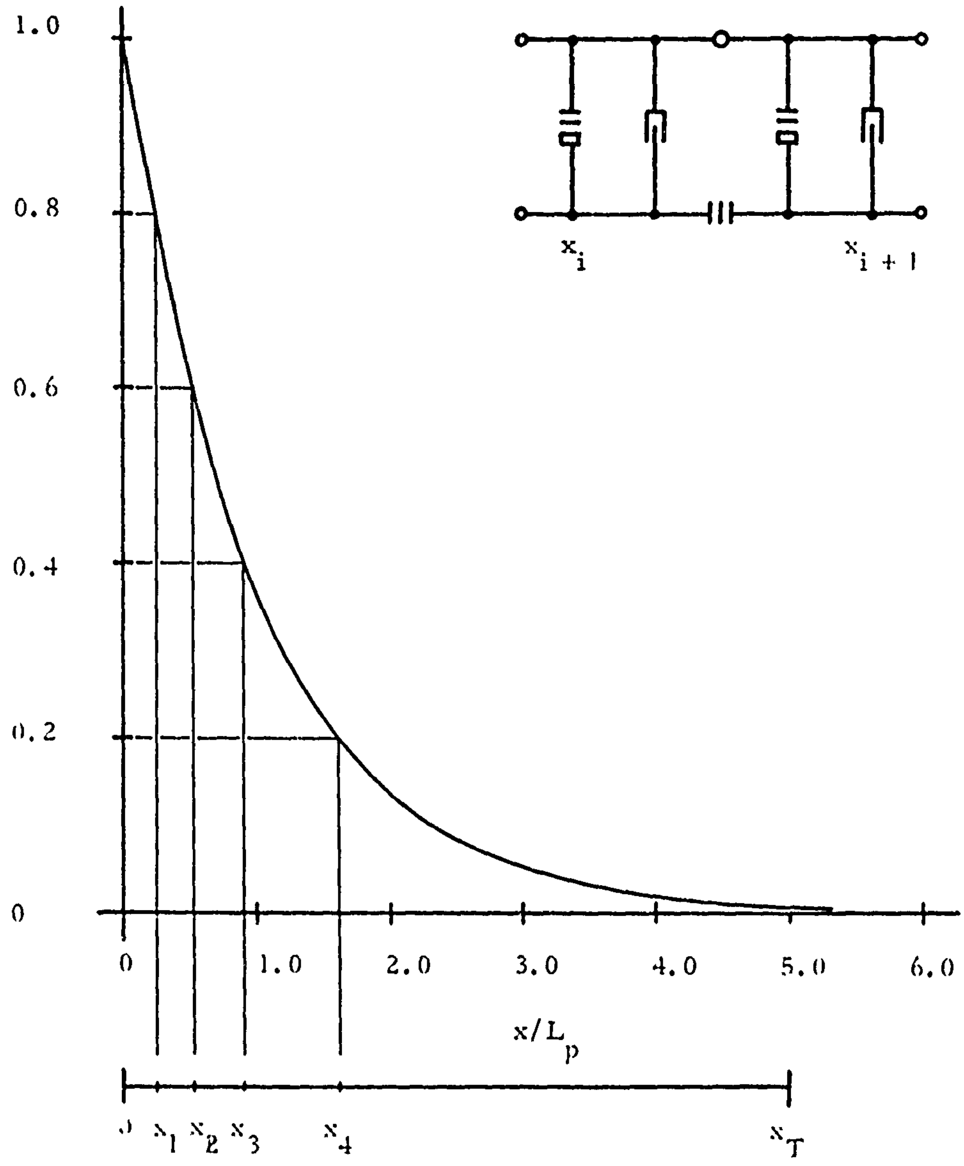


Figure 14

P-N Junction Diode Example Circuit



Exponential Definition of Lump Geometries

Figure 15

```
      PROGRAM LUMP(INPUT,OUTPUT,TAPE5=INPUT,TAPE6=OUTPUT)
C     COMPUTES PI-SECTION LUMPED MODEL PARAMETERS
C     FOR A SEMICONDUCTOR REGION USING A ONE DIMENSIONAL
C     EXPONENTIALLY VARYING GEOMETRY
C
C     A THREE LUMP MODEL LOOKS LIKE THIS
C
C      HD1      HD2             HD3
C     /-----/----------/-------------------/
C     + W1  +    W2    +        W3         +
C     P1    P2         P3                  P4=0
C     DX1   DX2        DX3
C
      REAL LP,LT
2     FORMAT(1H1,1X,I3,* LUMP P-N JUNCTION PI MODEL PARAMETERS*,//,
     *2X,*Q = *,E10.3,*  A= *,E10.3,*  L= *,E10.3,* TAU= *,E10.3,/,
     **  DP= *,E10.3,*  LT= *,E10.3)
3     FORMAT(1X,* DX= *,E12.4,*  HC*,I2,,2X,*  0  P*,I2,2X,E10.3,/,
     *1X,* W0= *,E12.4,*  ST*,I2,2X,*  0  P*,I2,2X,E10.3,/,
     *1X,* W1= *,E12.4,*  HD*,I2,2X,*P*,I2,*  P*,I2,2X,E10.3,/)
4     FORMAT(1X,* LENGTH TO P*,I2,* NODE= *,E12.4)
C
C     INPUTS TO DEFINE THE JUNCTION GEOMETRY ARE
C     A....JUNCTION AREA (CM**2)
C     TAU..MINORITY CARRIER LIFETIME (NSEC)
C     DP...MINORITY CARRIER DIFFUSION CONSTANT
C     N....NUMBER OF LUMPED REGIONS
C
      A=1.E-3
      TAU=100.
      DP=13.0E-9
      N=5
C
C     OUTPUTS ARE
C     L....MINORITY CARRIER DIFUSION LENGTH  (CM)
C     LT...LENGTH OF SEMICONDUCTOR REGION (CM)
C          LT IS 3*L FOR (N.LE.4)
C          LT IS 5*L FOR (N.GT.4 BUT .LE.7)
C          LT IS 10*L FOR (N.GT.7)
C     VALUES OF COMBINANCES STORANCES AND DIFFUSANCES ARE COMPUTED
C     FOR INPUT TO NET-2
C
      Q=1.6E-7
      X=0.0
      LP=SQRT(DP*TAU)
      LT=10.0*LP
      IF(N.LE.7) LT=5.0*LP
      IF(N.LE.4) LT=3.0*LP
      W0=0.0
      WD=0.0
      DY=1.0/N
      WRITE(6,2) N,Q,A,LP,TAU,DP,LT
      DO 10 I=1,N
      WD=WD+W0
      IF(N.NE.I) W1=-ALOG(FLOAT(N-I)*DY)-WD
      IF(N.EQ.I) W1=LT/LP-WD
      DX=LP*(W0+W1)/2.0
      HC=Q*A*DX/TAU
      ST=Q*A*DX
      HD=Q*A*DP/(W1*LP)
      K=I+1
      X=X+W1*LP
      WRITE(6,4) I,X
      WRITE(6,3) DX,I,I,HC,W0,I,I,ST,W1,I,I,K,HD
10    W0=W1
      STOP
      END
```

Figure 16

Computer Program for Computation of Pi-section Lumps for a Semiconductor Region.

```
5 LUMP P-N JUNCTION PI MODEL PARAMETERS

Q =   1.600E-07   A=   1.000E-03   L=   1.140E-03 TAU=   1.000E+02
DP=   1.300E-08   LT=   5.701E-03
LENGTH TO P 1 NODE=    2.5442E-04
DX=    1.2721E-04   HC 1      0   P 1    2.035E-16
W0=    0.           ST 1      0   P 1    2.035E-14
W1=    2.2314E-01   HD 1   P 1    P 2    8.175E-15

LENGTH TO P 2 NODE=    5.8243E-04
DX=    2.9122E-04   HC 2      0   P 2    4.659E-16
W0=    2.2314E-01   ST 2      0   P 2    4.659E-14
W1=    2.8768E-01   HD 2   P 2    P 3    6.341E-15

LENGTH TO P 3 NODE=    1.0447E-03
DX=    3.9515E-04   HC 3      0   P 3    6.322E-16
W0=    2.8768E-01   ST 3      0   P 3    6.322E-14
W1=    4.0547E-01   HD 3   P 3    P 4    4.499E-15

LENGTH TO P 4 NODE=    1.8350E-03
DX=    6.2631E-04   HC 4      0   P 4    1.002E-15
W0=    4.0547E-01   ST 4      0   P 4    1.002E-13
W1=    6.9315E-01   HD 4   P 4    P 5    2.632E-15

LENGTH TO P 5 NODE=    5.7009E-03
DX=    2.3281E-03   HC 5      0   P 5    3.725E-15
W0=    6.9315E-01   ST 5      0   P 5    3.725E-13
W1=    3.3906E+00   HD 5   P 5    P 6    5.380E-16
```

Figure 17

The Computed Pi-section Parameters for the 5-Lump Diode

```
*LUMP MODEL DIODE PHOTORESPONSE
LIBRARY
    PN PNBT 8
        C 0.1
        NPO 1+2
        PNO 1+5
        N 0
        TH 40
        VZ 0.7
V1 1 0 10
R1 1 C 0
PN1 A C N1 P1 PNBT
R2 A 0 1-4
P1 0
F1(A,B,C) =(A*B*C)
TABLE1
    0 1
    0.1 0
HC1 C P1 2.035-16
ST1 C P1 2.035-14
HD1 P1 P2 8.175-15
HC2 C P2 4.659-16
ST2 C P2 4.659-14
HD2 P2 P3 6.341-15
HC3 C P3 6.322-16
ST3 C P3 6.322-14
HD3 P3 P4 4.499-15
HC4 C P4 1.002-15
ST4 C P4 1.002-13
HD4 P4 PF 2.632-15
HC5 C PF 3.725-15
ST5 C PF 3.725-13
HD5 PF C 5.380-16
I1 P1 C F1(P1,4+15,2.035-16)*TABLE1(TIME)
I2 P2 C F1(P1,4+15,4.659-16)*TABLE1(TIME)
I3 P3 C F1(P1,4+15,6.322-16)*TABLE1(TIME)
I4 P4 C F1(P1,4+15,1.002-15)*TABLE1(TIME)
I5 PF C F1(P1,4+15,3.725-15)*TABLE1(TIME)
STATE1
    R1 1-2
    P1 1
    TIME 0 (100) 100 (50) 200 (20) 400
    PLOT I(R1)
    PRINT I(R1) N(C) N(P1) N(P2) N(PF)
STATE2
    R1 10
    TIME 0 (100) 100 (50) 200 (20) 400
    *P1 0.1 0.2 0.5 1.0 4.0 10 0 40.0 100.0
    PLOT I(R1)
    PLOT N(P1)
    PRINT I(R1) N(C) N(P1) N(P2) N(PF)
END
```

Figure 18

NET-2 Input Deck for the 5-Lump Diode Example.

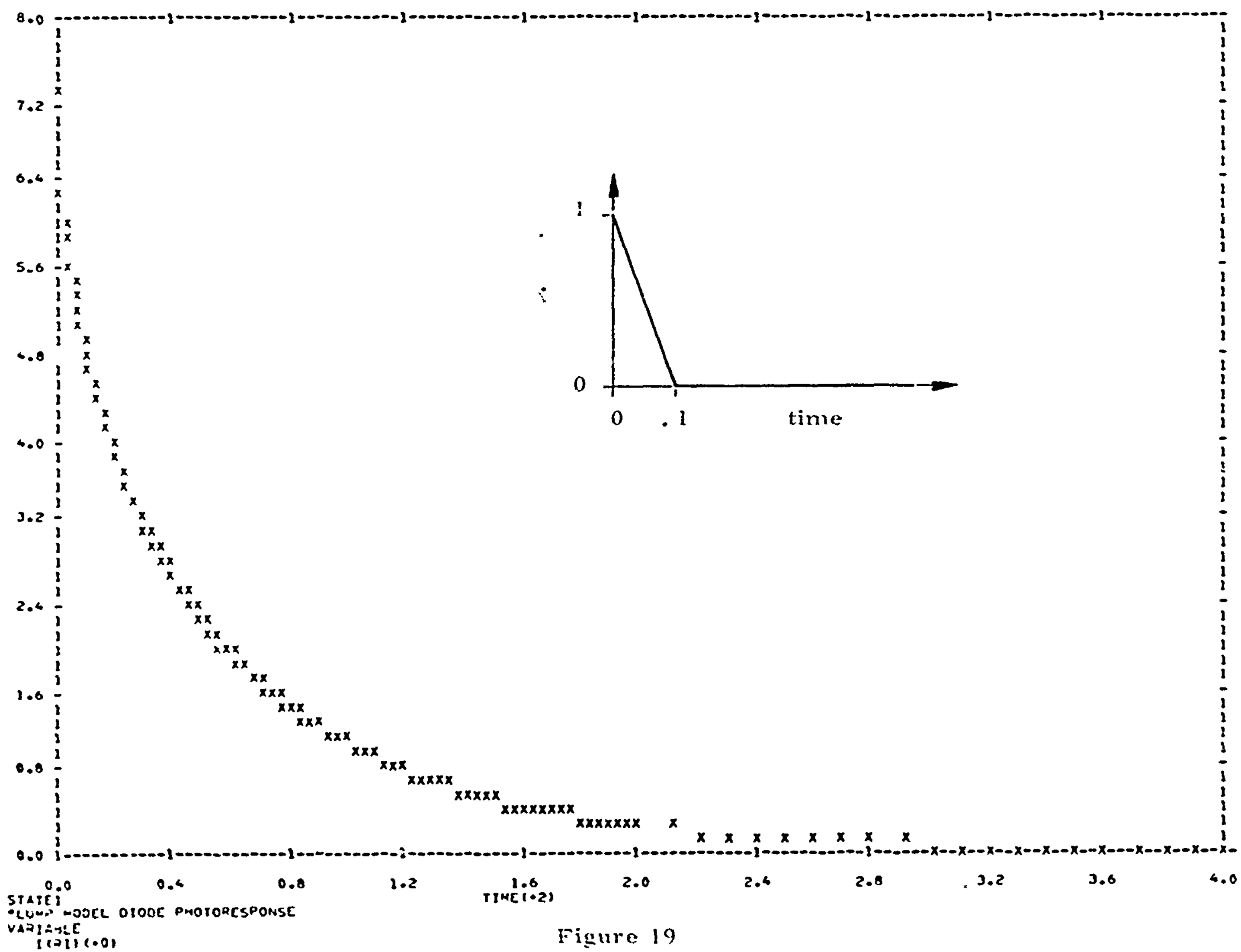


Figure 19

Computed Response to a Step Photocurrent

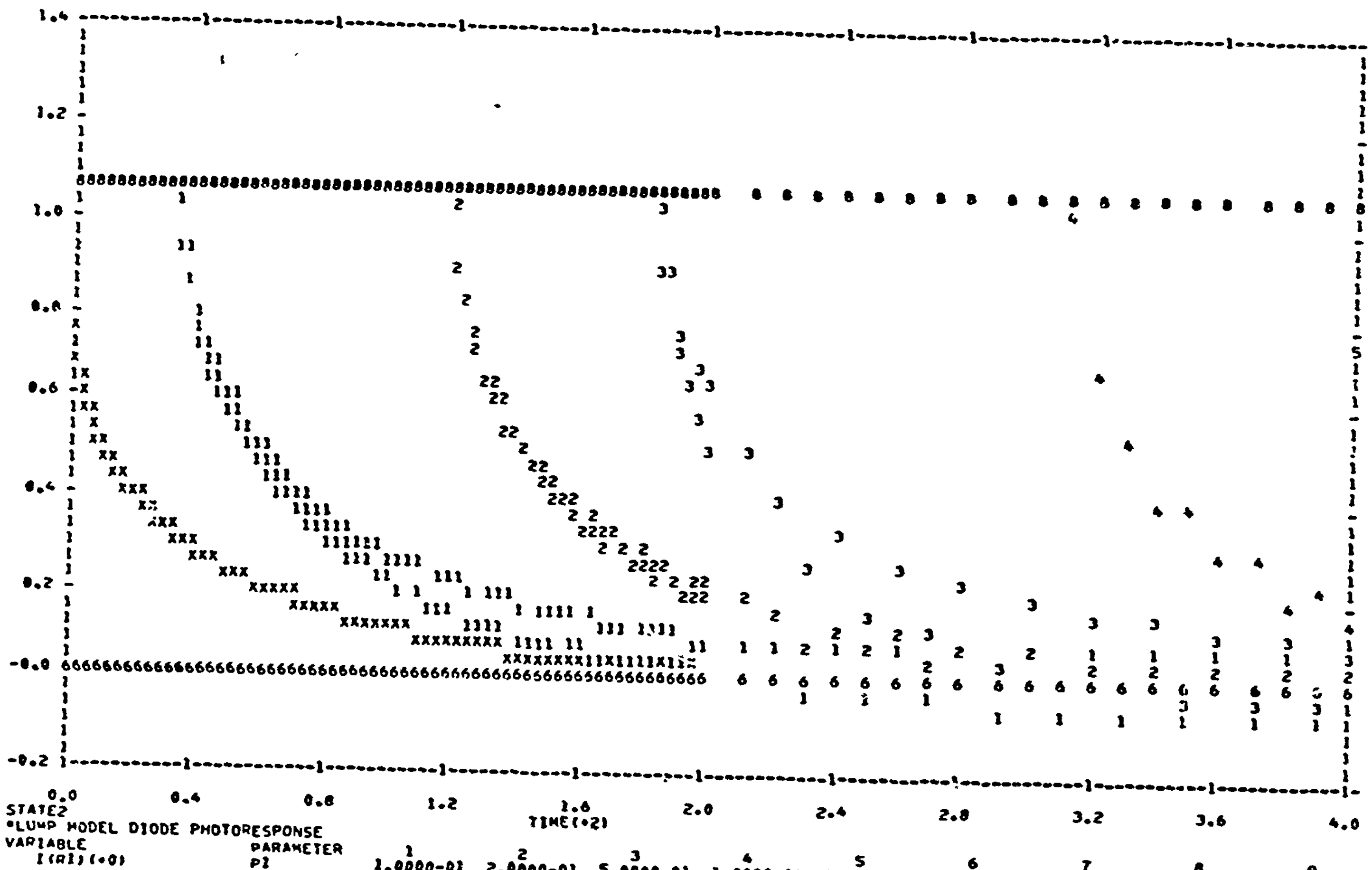


Figure 20

NET-2 Computed Transient Responses Representing Radiation-Induced Diode Saturation and Recovery for Variable I (R1)

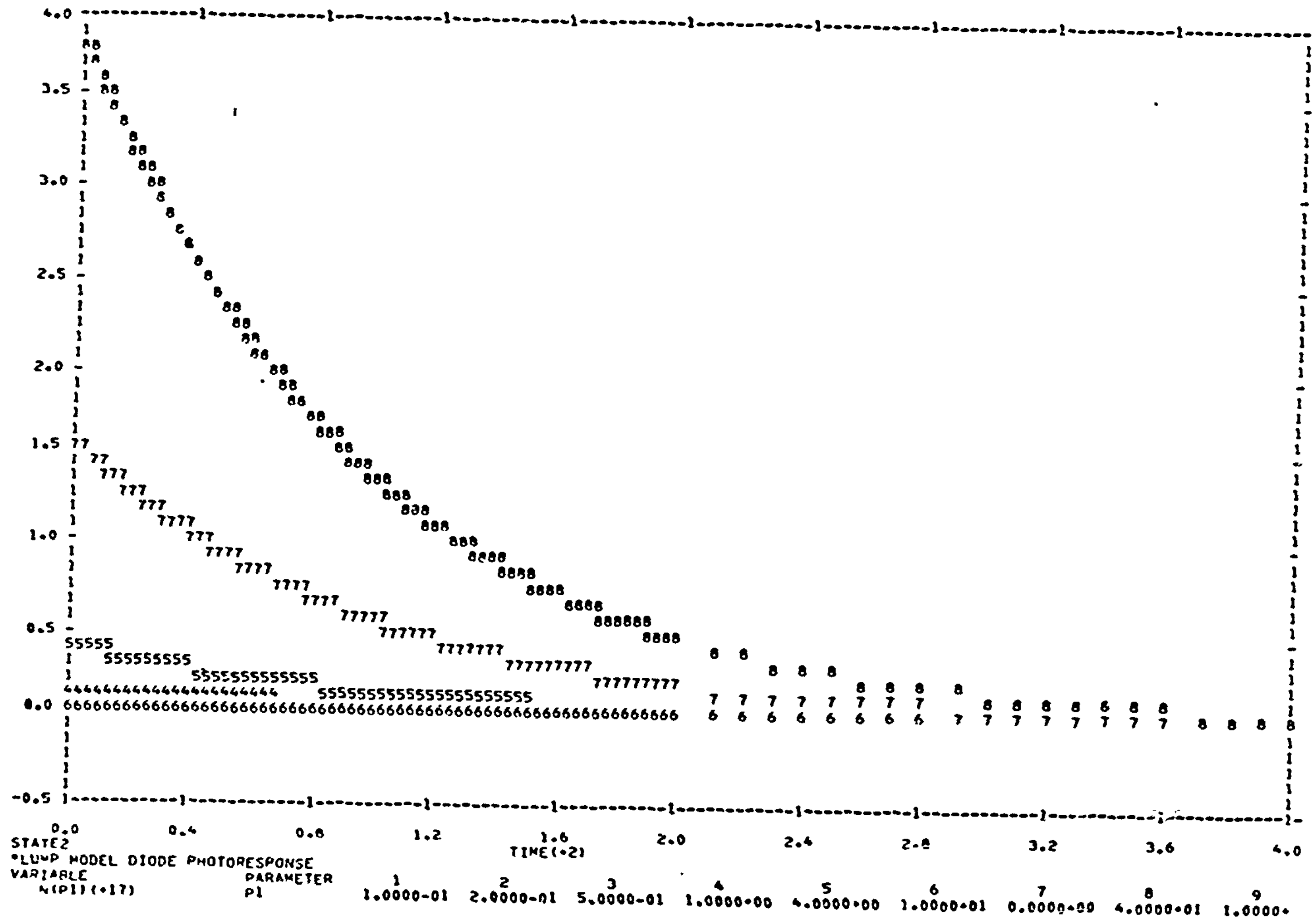


Figure 21

NET-2 Computed Transient responses Representing Radiation-Induced Diode Saturation and Recovery for Variable N(PI)

4.2 Intrinsic Lumped Model Transistor Analysis Example

The transistor model considered for this example is shown in Figure 22. It consists of a 1-lump base region with a built-in electric field and an exponentially spaced 4-lump collector. The 1-lump base region representation alone is equivalent to the basic Ebers-Moll model.

The NET-2 input deck for the circuit is shown in Figure 23. State 1 produced a calculation of the transistor small signal switching response. The switching time constant was computed to be 32 nanoseconds with DF31 = 0, thus $f_\beta = 5$ MHZ. With the driftance element connected as shown and with a positive value the effect was a decrease in transistor current gain. The same connection and a negative value yields an aiding field, thus, an increase in current gain. The State 2 calculation produced a frequency response with both aiding and retarding electric field. The computation gave the following results for the gain bandwidth product, f_T.

DF31		f_T
0	no field	500 MHz
2.6-15	retarding field	250 MHz
-5.2-15	aiding field	1000 MHz

```
*LUMPED MODEL TRANSISTOR ANALYSIS
LIBRARY
 PN PNBE B
  C 3.0
  NPO 1.2+3
  PNO 1.2+2
  N 0.5
  VZ 0.7
  TH 40.0
 PN PNBC B
  C 1.0
  NPO 1.2+5
  PNO 1.2+5
  N 0.33
  VZ 0.7
  TH 40.0
I100 B 0 TABLE1(TIME)
TABLE1
 0 0.01
 1 0.011
V1 1 0 10
R1 E 0 0.001
R2 1 C 0.001
HC1 C P1 9.464-18
HC2 C P2 2.281-17
HC3 C P3 3.614-17
HC4 C P4 6.841-17
ST1 C P1 9.464-16
ST2 C P2 2.281-15
ST3 C P3 3.614-15
ST4 C P4 6.841-15
HD1 P1 P2 1.754-15
HD2 P2 P3 1.247-15
HD3 P3 P4 7.297-16
HD4 P4 C 3.649-16
PN2 B C N32 P1 PNBC
HC31 B N31 5.200-17
HC32 B N32 5.200-17
ST31 B N31 3.200-16
ST32 B N32 3.200-16
HD31 N32 N31 5.200-15
DF31 N31 N32 0.0
PN1 B E N31 P41 PNBE
STATE1
 TIME 0 (100) 200
 *DF31 5.2-16 0.0 -5.2-15
 PLOT N(B) N(E) N(C)
 PRINT N(B) N(E) N(C) I(V1) N(P1) N(N31)
STATE2
 I100 0.01
 FREQ 1-5 (30*) 1
 *DF31 2.6-15 -5.2-15
 PRINT B(C-0/B-0)
END
```

Figure 23

NET-2 Input Deck for the Lumped Model Transistor Analysis Example.

SECTION 5.0

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

The overall conclusion of this study is that NET-2 can be an efficient, cost-effective aid to engineering semiconductor device/microcircuit analysis of electrical performance and radiation effects.

Many suggestions arising during the course of the study have already been implemented in NET-2. No matter how great any analysis aid is now, there is always more we could hope for. These include:

1) Avalanche breakdown effects in the p-n junction model to enable direct model formulation of p-n-p-n diodes, SCR's and pulsed electrical overstress effects.

2) Variation of combinance with carrier density (i.e., $H_{ck} = f(p_k)$) to enable representation of variation of transistor gain with injection level.

3) Variation of driftance with carrier density to represent more general electric field effects.

4) Representation of majority carrier current flow as well as minority carrier effects to allow convenient analysis of majority carrier devices (junction FET's, MOS transistors).

The implementation of these suggestions is not necessary to give NET-2 a device analysis capability, but will extend existing capability.